Data Sheet | November 3, 2005 | FN6190.0

Ultra Low ON-Resistance, Low Voltage, Single Supply, Dual SPDT Analog Switch in Chipscale Package

The Intersil ISL84684II device is a low ON-resistance, low voltage, bidirectional, dual single-pole/double-throw (SPDT) analog switch designed to operate from a single +1.8V to +4.5V supply. Targeted applications include battery powered equipment that benefit from low R_{ON} (0.21Ω) and fast switching speeds (t_{ON} = 43ns, t_{OFF} = 27ns). The digital logic input is 1.8V logic-compatible when using a single +1.8V to 4.5V supply.

Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This part may be used to “mux-in” additional functionality while reducing ASIC design risk. The ISL84684II is offered in a 2.00mm x 1.50mm chipscale package, alleviating board space limitations. The 4x3 array of solder balls are spaced with a 0.5mm ball pitch.

The ISL84684II is a committed dual single-pole/double-throw (SPDT) that consist of two normally open (NO) and two normally closed (NC) switches. This configuration can be used as a dual 2-to-1 multiplexer. The ISL84684II is pin compatible with the MAX4684 and MAX4685.

TABLE 1. FEATURES AT A GLANCE

	ISL84684II
Number of Switches	2
SW	SPDT or 2-1 MUX
2.7V R_{ON}	0.21Ω
2.7V t_{ON}/t_{OFF}	43ns/27ns
4.3V R_{ON}	0.14Ω
4.3V t_{ON}/t_{OFF}	30ns/25ns
Package	10 ball, 2.0mm x 1.5mm depopulated 4x3 array Chipscale

Related Literature

- Technical Brief TB451 “PCB Assembly Guidelines for Intersil Wafer Level Chip Scale Package Devices”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

Features

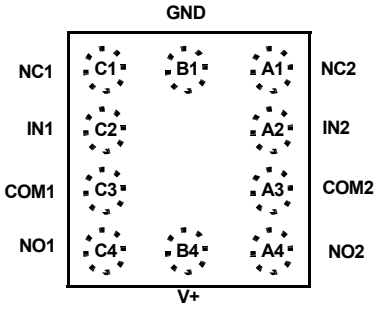
- Pb-Free Plus Anneal Available (RoHS Compliant)
- Pin Compatible Replacement for the MAX4684 and MAX4685
- ON Resistance (R_{ON})
  - V+ = +2.7V 0.21Ω
  - V+ = +4.3V 0.14Ω
- R_{ON} Matching Between Channels, maximum 0.05Ω
- R_{ON} Flatness Across Signal Range, maximum 0.03Ω
- Single Supply Operation . . . . . +1.8V to +4.5V
- Low Power Consumption P_D . . . . . <0.32µW
- Fast Switching Action (V+ = +2.7V)
  - t_{ON} 43ns
  - t_{OFF} 27ns
- Guaranteed Break-before-Make
- 1.8V Logic Compatible
- Low I+ Current when VinH is not at the V+ Rail
- Available in 10 ball 4x3 Array Chipscale Package (2mm x 1.5mm)

Applications

- Battery powered, Handheld, and Portable Equipment
  - Cellular/mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio and Video Switching

Pinout (Note 1)

ISL84684II (CHIPSCALE)
TOP VIEW



NOTE:

1. B2 and B3 of the 4x3 array are not populated.

Truth Table

LOGIC	PIN NC1 and NC2	PIN NO1 and NO2
0	ON	OFF
1	OFF	ON

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+1.8V to +4.5V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin

Ordering Information

PART NO.	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL84684IIZ-T (Note)	684Z	-40 to 85	10 ball, 2.0mm x 1.5mm, depopulated 4x3 array, Chipscale Pb-free, Tape and Reel	W4x3.10A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to +5V
Input Voltages
NO, NC, IN (Note 2) . . . . . -0.3 to ((V+) + 0.3V)
Output Voltages
COM (Note 2) . . . . . -0.3 to ((V+) + 0.3V)
Continuous Current NO, NC, or COM . . . . . ±300mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±500mA
ESD HBM rating (Per Mil-Std-883, Method 3015) . . . . . ±2kV

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
10 Ball Chipscale Package	91

Maximum Storage Temperature Range . . . . . -65°C to 150°C
Soldering conditions (Note 4) . . . . . per J-STD-020

Operating Conditions

Temperature Range
ISL84684II . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Signals on NC, NO, IN, or COM exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. Permitted soldier profiles are limited to only those recommended in the industry standard specification, JEDEC J-STD-020. Preheating is required. Hand or wave soldering is not allowed. See Technical Brief TB451.

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Notes 5, 7) Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 6) MIN	TYP	(NOTE 6) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (See Figure 5, Note 9)	25	-	0.21	0.5	Ω
		Full	-	-	0.5	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max R_{ON} (Note 9, Note 10)	25	-	0.05	0.06	Ω
		Full	-	-	0.09	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (Note 8, Note 9)	25	-	0.03	0.2	Ω
		Full	-	-	0.2	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, V_{NO} or V_{NC} = 3V, 0.3V	25	-40	-	40	nA
		Full	-150	-	150	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, or V_{NO} or V_{NC} = 0.3V, 3V, or Floating	25	-40	-	40	nA
		Full	-150	-	150	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 9)	25	-	43	50	ns
		Full	-	-	60	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 9)	25	-	27	30	ns
		Full	-	-	40	ns
Break-Before-Make Time Delay, t_D	V+ = 3.3V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 3, Note 9)	Full	2	12	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2)	25	-	200	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, (See Figure 4)	25	-	56	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, (See Figure 6)	25	-	-105	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 32Ω	25	-	0.012	-	%
	f = 1kHz, V_{COM} = $2V_{P-P}$, R_L = 32Ω	25	-	0.009	-	%
	f = 1kHz, V_{COM} = $2V_{P-P}$, R_L = 600Ω	25	-	0.006	-	%
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	140	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	355	-	pF

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Notes 5, 7) Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 6) MIN	TYP	(NOTE 6) MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.8	-	4.5	V
Positive Supply Current, I+	V+ = +4.5V, V_{IN} = 0V or V+	25	-	5	20	nA
		Full	-	-	70	nA
Positive Supply Current, I+	V+ = +4.2V, V_{IN} = 2.85V	25	-	1.6	4	µA
		Full	-	-	8	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V_{IN} = 0V or V+ (Note 9)	Full	-0.5	-	0.5	µA

NOTES:

5. V_{IN} = input voltage to perform proper function.
6. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
7. Parts are 100% tested at +25°C. Limits across the full temperature range are guaranteed by design and correlation.
8. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
9. Guaranteed but not tested.
10. R_{ON} matching between channels is calculated by subtracting the channel with the highest max R_{ON} value from the channel with lowest max R_{ON} value.

Electrical Specifications - 4.3V Supply

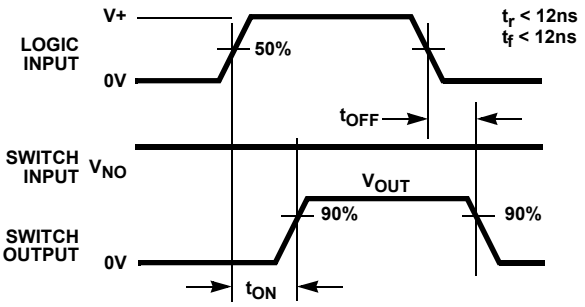
Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Notes 5, 7), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 6) MIN	TYP	(NOTE 6) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 3.9V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (See Figure 5)	25	-	0.14	-	Ω
		Full	-	0.17	-	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 3.9V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max R_{ON} (Note 10)	25	-	0.05	-	Ω
		Full	-	0.06	-	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3.9V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (Note 8)	25	-	0.03	-	Ω
		Full	-	0.04	-	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 4.5V, V_{COM} = 0.3V, 3V, V_{NO} or V_{NC} = 3V, 0.3V	25	-	0.9	-	µA
		Full	-	4	-	µA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 4.5V, V_{COM} = 0.3V, 3V, or V_{NO} or V_{NC} = 0.3V, 3V, or Floating	25	-	0.9	-	µA
		Full	-	4	-	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 3.9V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 9)	25	-	30	40	ns
		Full	-	-	45	ns
Turn-OFF Time, t_{OFF}	V+ = 3.9V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 9)	25	-	25	35	ns
		Full	-	-	40	ns
Break-Before-Make Time Delay, t_D	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (See Figure 3, Note 9)	Full	2	4	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2)	25	-	260	-	pC

Electrical Specifications - 4.3V Supply Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Notes 5, 7), Unless Otherwise Specified **(Continued)**

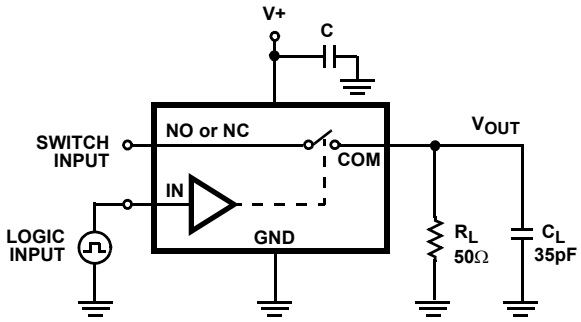
PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 6) MIN	TYP	(NOTE 6) MAX	UNITS
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = 1V_{RMS}, (See Figure 4)	25	-	56	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = 1V_{RMS}, (See Figure 6)	25	-	-105	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	140	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	355	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.8	-	4.5	V
Positive Supply Current, I+	V+ = +4.5V, V_{IN} = 0V or V+	25	-	5	20	nA
		Full	-	-	70	nA
Positive Supply Current, I+	V+ = +4.2V, V_{IN} = 2.85V	25	-	1.6	4	µA
		Full	-	-	8	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 4.5V, V_{IN} = 0V or V+ (Note 9)	Full	-0.5	-	0.5	µA

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

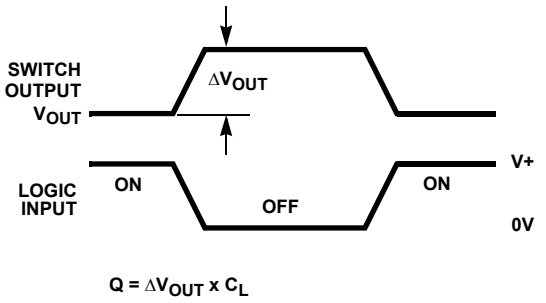
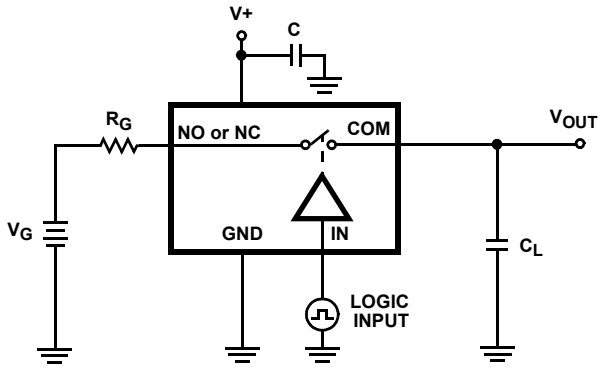


FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches.

FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

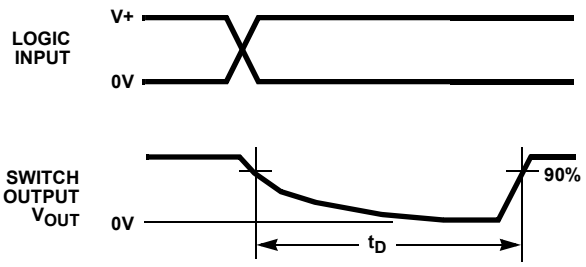
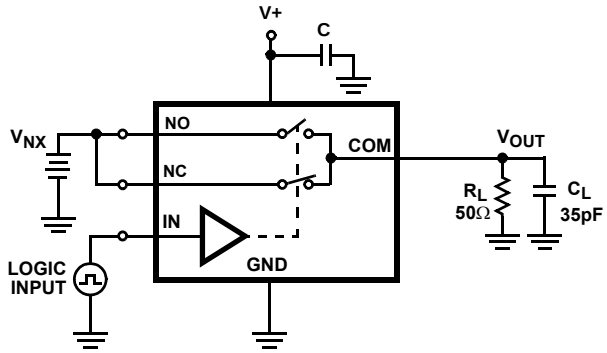


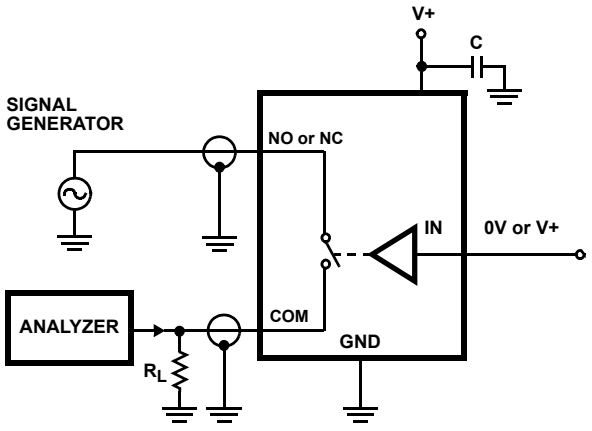
FIGURE 3A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

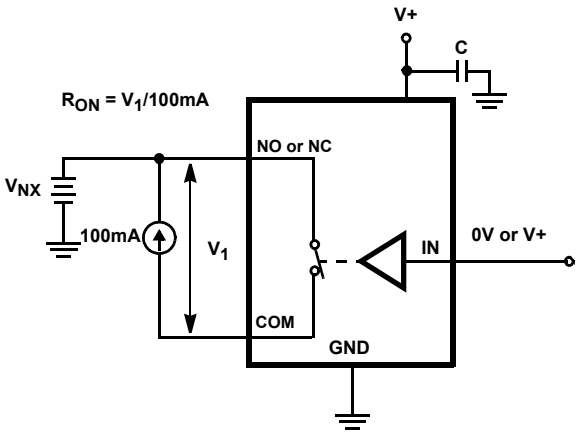
FIGURE 3B. TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

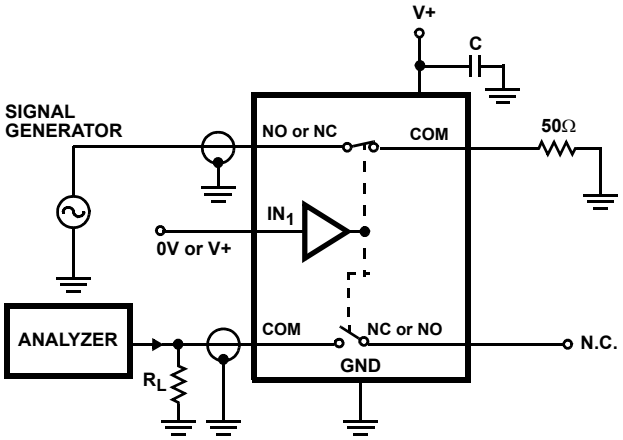
FIGURE 4. OFF ISOLATION TEST CIRCUIT



Repeat test for all switches.

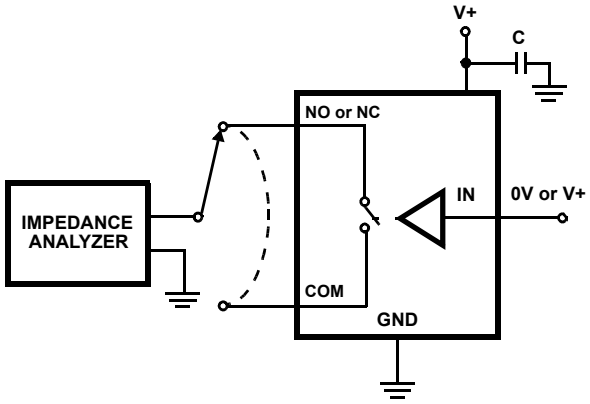
FIGURE 5. R_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 6. CROSSTALK TEST CIRCUIT



Repeat test for all switches.

FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL84684II is a bidirectional, dual single pole/double throw (SPDT) analog switch that offers precise switching capability from a single 1.8V to 4.5V supply with low on-resistance (0.21Ω) and high speed operation (t_{ON} = 43ns, t_{OFF} = 27ns). The device is especially well suited for portable battery powered equipment due to its low operating supply voltage (1.8V), low power consumption (0.32µW max), low leakage currents (150nA max), and the tiny chipscale package. The ultra low on-resistance and R_{ON} flatness provide very low insertion loss and distortion to applications that require signal reproduction.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provide additional protection to limit the current in the event that the voltage at a signal pin or logic pin goes below ground or above the V+ rail.

Logic inputs can be protected by adding a 1kΩ resistor in series with the logic input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch. Connecting schottky diodes to the signal pins as shown in Figure 8 will shunt the fault current to the supply or to ground thereby protecting the switch. These schottky diodes must be sized to handle the expected fault current.

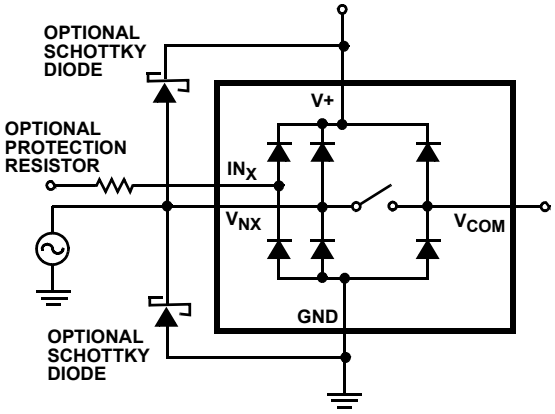


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL84684II construction is typical of most single supply CMOS analog switches, in that they have two supply pins; V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL84684II 5V maximum supply voltage provides plenty of room for the 10% tolerance of a 4.3V supply, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.8V but the part will operate with a supply below 1.5V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance* curves for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 1.8V to 4.5V (see Figure 16). At 4.5V the V_{IH} level is about 1.3V. This is still below the 1.8V CMOS guaranteed high output minimum level of 1.4V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation. The ISL84684II has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example driving the device with 2.85V logic (0V to 2.85V) while operating with a 4.2V supply the device draws only 1.6µA of current.

High-Frequency Performance

In 50Ω systems, the signal response is reasonably flat even past 10MHz with a -3dB bandwidth of 80MHz (see Figure 17). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off Isolation is the resistance to this feedthrough, while Crosstalk indicates the amount of feedthrough from one switch to another. Figure 18 details the high Off Isolation and Crosstalk rejection provided by this part. At 100kHz, Off Isolation is about 56dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified

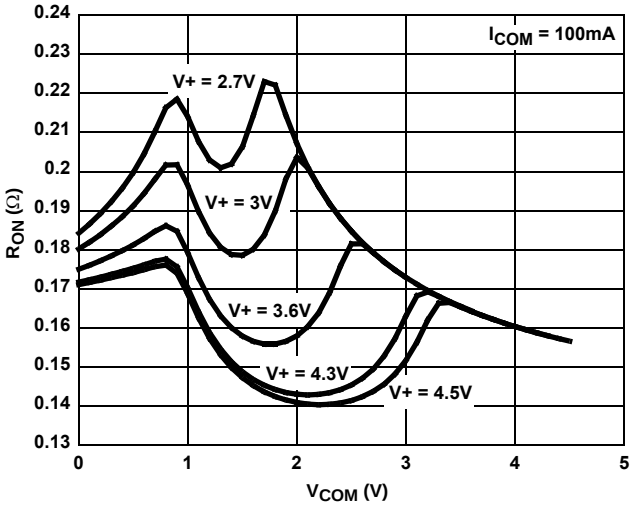


FIGURE 9. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

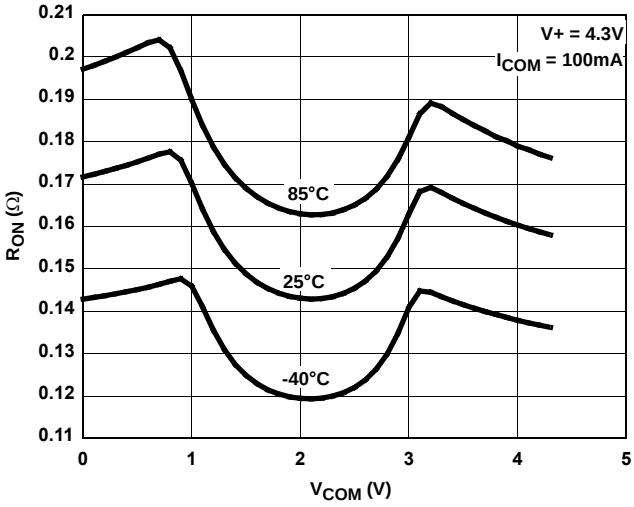


FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

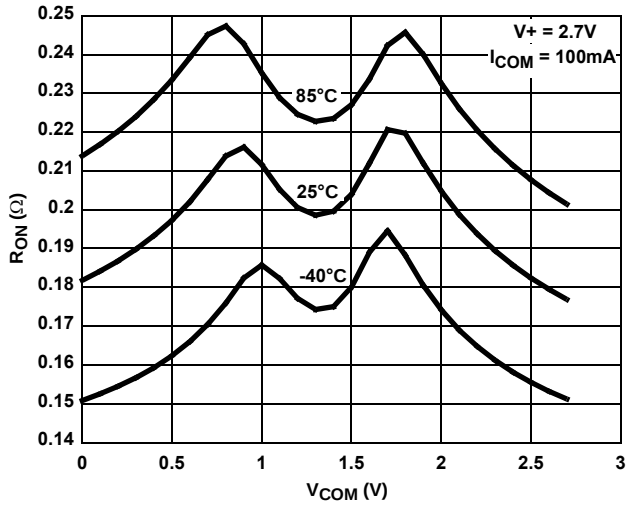


FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

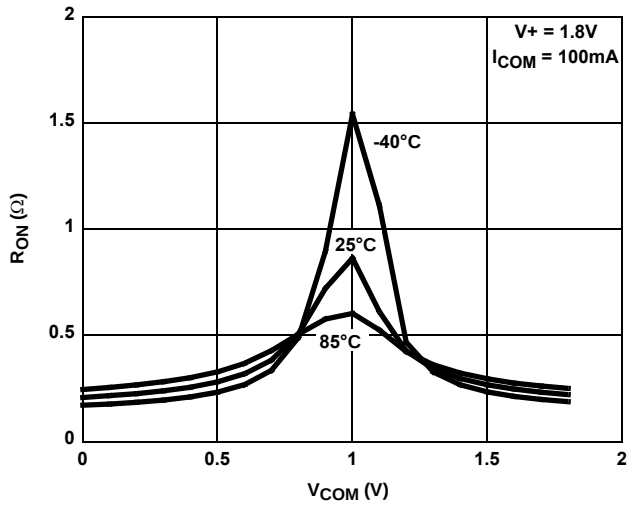


FIGURE 12. ON RESISTANCE vs SWITCH VOLTAGE

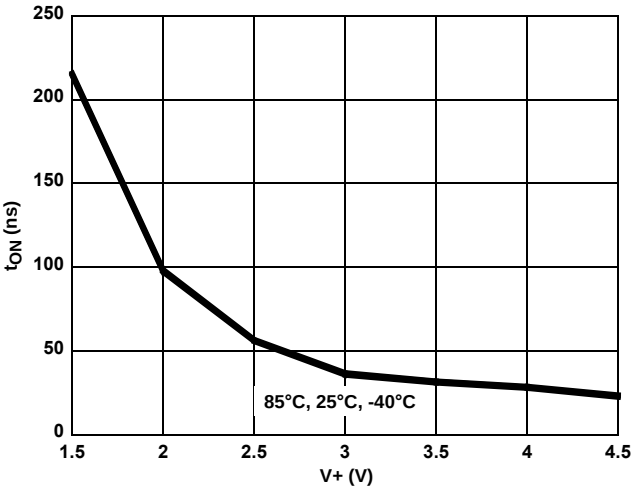


FIGURE 13. TURN-ON TIME vs SUPPLY VOLTAGE

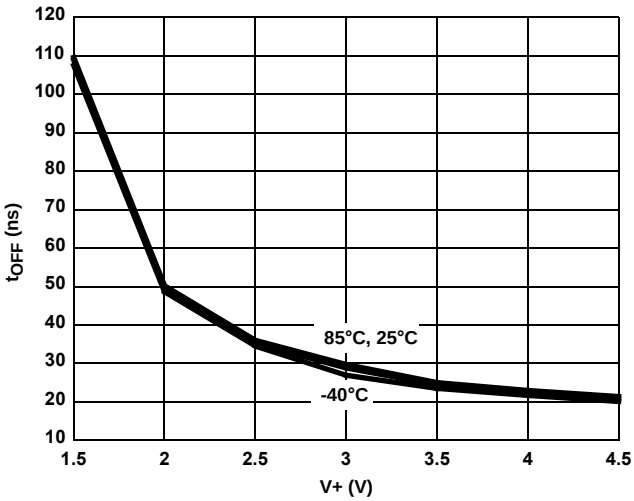


FIGURE 14. TURN-OFF TIME vs SUPPLY VOLTAGE

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

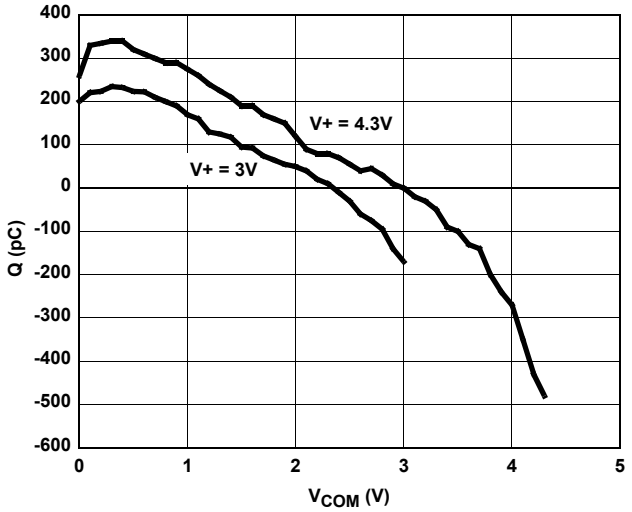


FIGURE 15. CHARGE INJECTION vs SWITCH VOLTAGE

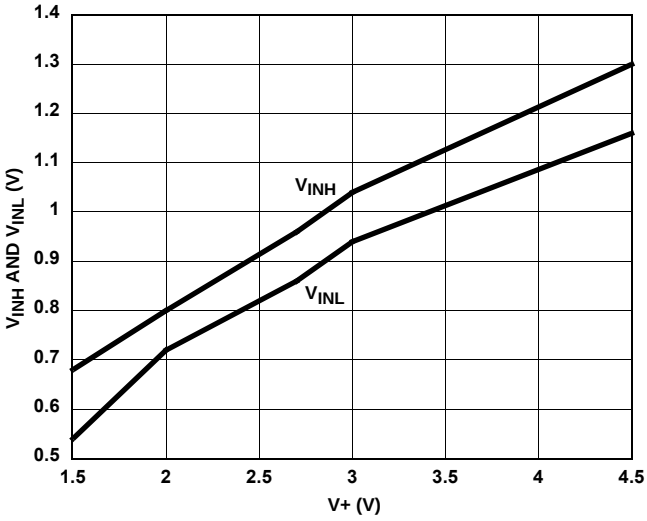


FIGURE 16. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

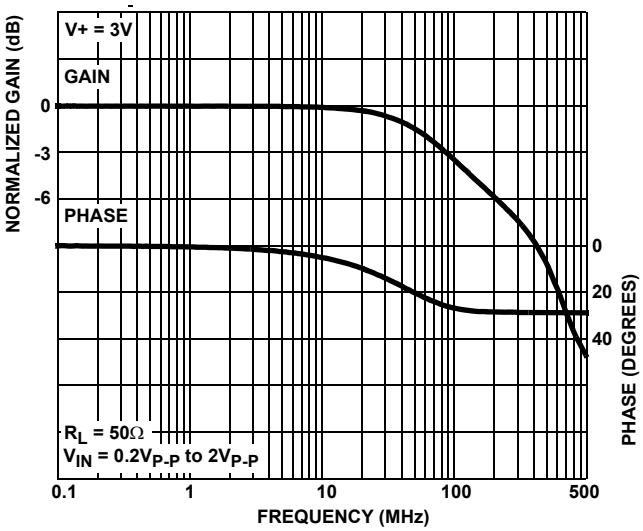


FIGURE 17. FREQUENCY RESPONSE

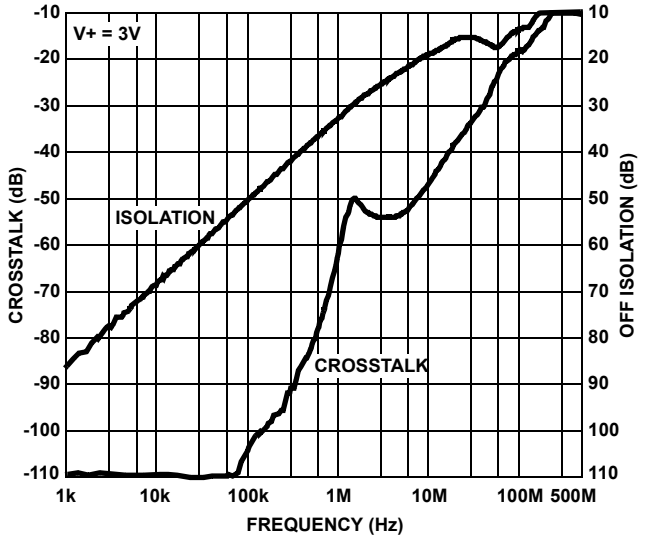


FIGURE 18. CROSSTALK AND OFF ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

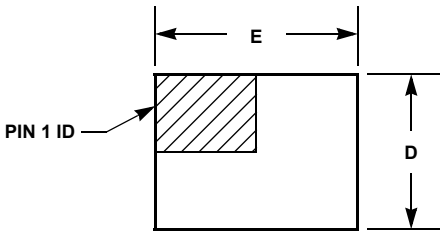
TRANSISTOR COUNT:

114

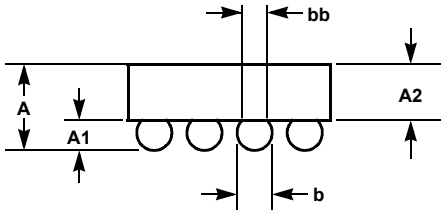
PROCESS:

Submicron CMOS

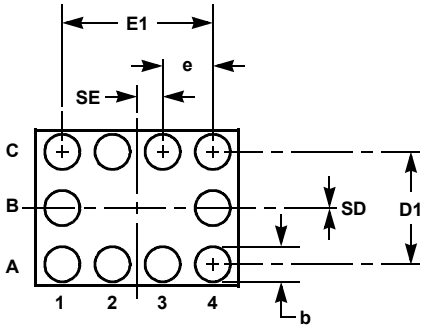
Wafer Level Chip Scale Package (WLCSP)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

W4x3.10A

4X3 ARRAY 10 BALL WAFER LEVEL CHIP SCALE PACKAGE

SYMBOL	MILLIMETERS	NOTES
A	0.64 +0.05 -0.10	-
A1	0.29 ±0.02	-
A2	0.35 REF.	-
b	θ 0.37 ±0.03	-
bb	θ 0.30 REF.	-
D	1.50 ±0.05	-
D1	1.00 BASIC	-
E	2.00 ±0.05	-
E1	1.50 BASIC	-
e	0.50 BASIC	-
SD	0.00 BASIC	-
SE	0.25 BASIC	-
N	10	3

Rev. 1 10/05

NOTES:

1. Dimensions are in Millimeters.
2. Dimensioning and tolerancing conform to ASME 14.5M-1994.
3. Symbol “N” is the actual number of solder balls.